

JITTER GENERATION AND MEASUREMENT FOR TEST OF MULTI-GBPS SERIAL IO

Sassan Tabatabaei
sassan@guidetech.com

Michael Lee
michael@guidetech.com

Freddy Ben-Zeev
freddy@guidetech.com

Guide Technology, 140 Kifer Court, Sunnyvale, CA 94086

Abstract

The advent of serial communication links in chip-to-chip and system-to-system applications has resulted in intense focus on jitter and BER testing techniques, including jitter generation and measurement methodologies. We describe techniques for injection of random and deterministic jitter in controlled and programmable fashion, including a novel data-dependent jitter (DDJ) generation method that eliminates the need for bulky and difficult-to-control DDJ injection filters. These techniques can be employed for a wide range of applications with different bit rates and patterns in a single setup. We also introduce the concept of continuous time interval analyzer (CTIA) and demonstrate how it can be used for fast and accurate jitter measurement without any trigger signal. Subsequently, we present jitter measurement methodologies and results using the real-time and equivalent-time sampling oscilloscopes, which are used as benchmarks for verification of the CTIA measurement accuracy.

1. Introduction

The continued market demand for GHz processors and high-capacity communication systems has resulted in an increasing number of low-cost high volume ICs clocked at GHz rates and beyond and/or equipped with multi-Gb/s serial interfaces, e.g., PCI-Express, Infiniband, HyperTransport, Serial ATA, etc. Circuits achieving such clock and/or data rates are characterized by very stringent timing specifications, often dictated by governing standards. Many of these standards specify maximum limits on jitter components such as random and deterministic for the transmitter (jitter generation) and minimum tolerable limits for the receiver (jitter tolerance) [1][2][3]. The purpose of specifying limits on jitter components is to provide faster ways to estimate the key performance parameter of bit-error-rate (BER), and to provide a

better interoperability measure when the devices are used in a system environment.

Jitter is generally divided into three components: random jitter (RJ), data-dependent jitter (DDJ), and periodic jitter (PJ) [2]. Each of these components is correlated with physical sources and impact bit error rate (BER) differently. Random jitter is typically due to the device noise sources, e.g., thermal and flicker noise, and is assumed unbounded with Gaussian distribution, while the combination of DDJ and PJ are bounded and can be traced back to deterministic sources such as transmission path bandwidth limitations, and cross-coupling. Qualifying a transmitter requires measurement of transmitter jitter components, while receiver testing necessitates generation of data streams with controlled amounts of RJ, DDJ, and PJ. This paper addresses methodologies for both jitter generation for receiver testing and jitter measurement for transmitter testing.

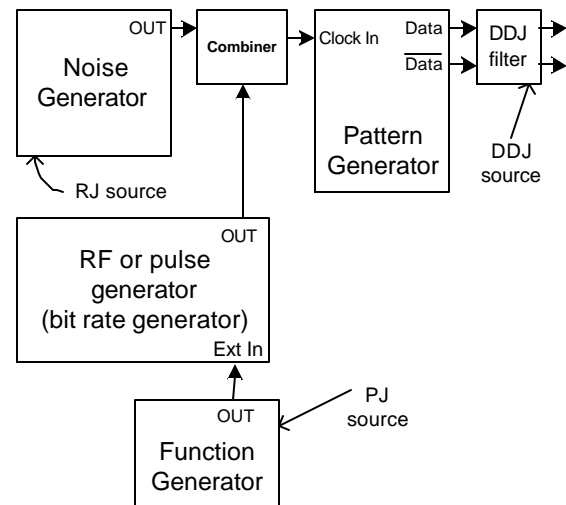


Figure 1: Typical RJ, DDJ, and PJ injection method

Figure 1 shows the typical test setup used for jitter injection, including in Xaui [1] and with a slight

modification for FiberChannel [2][4] tests. The RF generator is used as a stable clock source. The Noise generator output is superimposed on the clock signal to add random jitter. The low-pass multiple-pole filter [5], or long cable [6] is a source of DDJ. The FM or PM modulation capability of RF generator acts as a sinusoidal jitter source. This setup, although sufficient for some applications, lacks flexibility for use in multiple applications (requiring different bit rates and data patterns) because of the following issues:

1. Superimposition of random noise with RF signal works well as a RJ source only for small RJ injection (typically 0.02 UI). As the noise level is increased to generate larger RJ, the possibility of encountering spurious edges that would cause false edges away from the bit transition increases due to amplitude noise. Even the limiting amplifier specified in FiberChannel standard may not eliminate such sharp glitches. As shown in Figure 2, these false edges violate phase modulation conditions, which affect jitter measurement accuracy with varying degree depending on the measurement method used. In addition, the amount of injected jitter depends on the RF or pulse generator effective rise/fall time, which necessitates time-consuming calibration when testing different bit rates or test conditions.

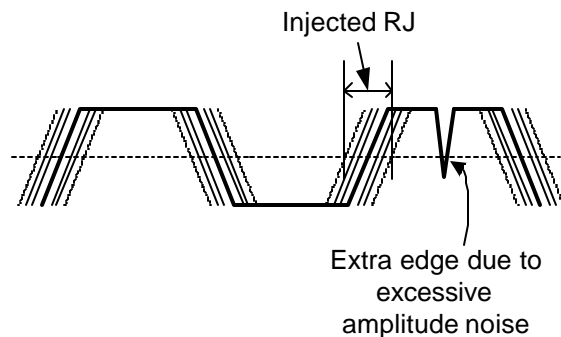


Figure 2: Extra edges due to large amplitude noise injection

2. The use of filters or long cables typically is limited to specific bit rates for a given amount of DDJ. Cables and filters have to be adjusted and calibrated for different bit rates specified for each IO standards.
3. Most RF generators are capable of low to medium frequency FM or PM modulation (typically less than 10MHz). However, in serial communication links, often the real PJ components that require

testing are due to coupling clock sources in the range of 20MHz to 400MHz.

We present a methodology based on delay-line phase modulation or direct timing synthesis that is capable of jitter injection with the following features:

- RJ injection with programmable RMS value without causing amplitude noise.
- Programmable amount of DDJ for any bit-rate and pattern. This novel technique replaces tunable filter with a programmable AWG, which enhances DDJ injection control and flexibility significantly.
- Both large amplitude (multiple UI) low frequency and low amplitude high frequency PJ injection.

To characterize transmitters and/or verify the jitter injection methods for receiver testing, jitter has to be decomposed to its subcomponents. A number of different methodologies have been proposed for jitter measurement, including using real-time (RT-) and equivalent-time (ET-) digital sampling oscilloscopes (DSO) [4][7][8], bit error rate testers [4], and time interval analyzers [9][10]. Jitter measurement with an oscilloscope typically takes several tens of second to minutes because many voltage samples must be taken to extract edge displacement information with sufficient accuracy, leading to long acquisition time in the case of the ET-DSO, or excessive processing time in the case of the RT-DSO. Time interval analyzers (TIA), on the other hand, provide the ability to optimize the sampling process by directly sampling edge timing, which results in much faster measurements. Traditional TIA are based on single-shot time interval measurement, in which each time interval is measured as the difference between a start and stop event. Such TIAs require a pattern marker/trigger signal for fast jitter decomposition.

In this paper, we introduce the concept of continuous time interval analyzer (CTIA) in which all the edge timings are measured relative to a common reference. The CTIA equipped with flexible and programmable arming modes allows implementation of fast and more flexible jitter measurement methodologies without the need for any hardware generated arming/trigger signal. This eliminates the need for the hardware clock recovery circuit, whose jitter can impact measurement results. Instead, the flexible event control mechanism provides an embedded or virtual marker capability that allows focused measurement of specific edges within a data stream. The CTIA fast measurements capability without any marker signal makes it a great candidate for production test of multi-Gbps IOs.

The rest of this paper is organized as follows. Section 2 discusses the delay-line based jitter generation methodology and proposes a technique for injection of a programmable amount of DDJ. In Section 3, we present methods for RJ and DDJ measurement using the CTIA that are precise, accurate, and yield high immunity of each measurement in the presence of other jitter types. Section 4 describes how to use RT-DSO and ET-DSO to verify the jitter content of a test signal. Section 5 presents results of injected jitter measurements taken with DSOs as reference and the CTIA. Finally, Section 6 presents the conclusions.

2. Controlled-Profile Jitter Injection

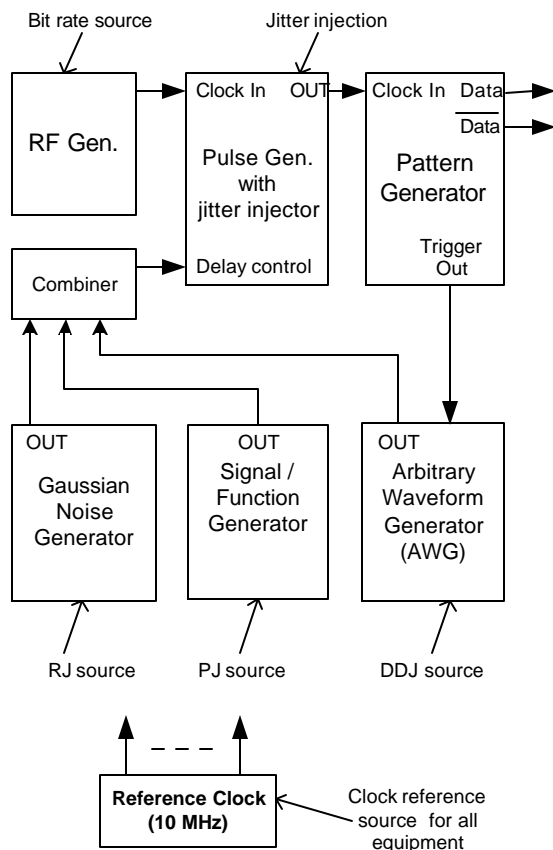


Figure 3: Proposed programmable jitter injection method

Our proposed jitter injection method is shown in Figure 3. An RF generator is used for low jitter bit clock generation. Subsequently, the controllable delay line within an Agilent 81133 pulse/pattern generator phase modulates the bit clock for jitter injection. The resulting “jittery” clock drives an Advantest D3186 pattern generator to provide a high-speed data with repeating pattern and controlled jitter. The NoiseCom PNG7109 noise generator, Agilent

8648A, and Tektronix AWG610 are used as RJ, PJ, and DDJ sources, respectively.

This setup provides two jitter injection mechanisms. The first is the PM modulation capability of the RF generator. This is primarily used to inject low frequency PJ with possibly multiple UI variation to test receiver tolerance to PJ up to a few MHz range. The second mechanism uses a delay line modulation approach, which effectively provides high bandwidth phase modulation. Agilent 81133 pulse/pattern generator includes such delay line. We use a combiner to add outputs of the noise generator, the sinusoidal signal source, and the arbitrary waveform generator (AWG). The combiner output drives the delay control input of the Agilent 81133 to inject jitter in the clock source.

The noise generator output is Gaussian noise with 1GHz bandwidth, which emulates a high bandwidth Gaussian random jitter as is specified in most standards. The signal generator acts as the PJ source, with capability to inject up to 500ps peak-to-peak periodic jitter. The AWG is used as a DDJ source for data signals with a repeated pattern. The AWG output is set such that its frequency is equal to the data bit rate divided by the pattern length in bits. In this fashion, effectively a periodic jitter is generated that is static relative to the pattern, which emulates the behavior of DDJ. A common 10MHz external reference is used to ensure that the sampling clock of the AWG is locked to the bit clock generator (the RF source). It is also essential to ensure phase consistency of the pattern relative to the AWG output to ensure that edge shift for each pattern edge is consistent from one repetition of the test to the next. Without such consistency, the AWG phase could be random relative to a specific edge of the pattern when the test starts, which will result in different DDJ reading for each repetition of the test. The phase consistency requirement is met through a combination of software and hardware trigger capabilities present in the Tektronix 610 AWG. This includes using the pattern trigger signal of the pattern generator to trigger the AWG output. Once the test is completed, software disables the output. Upon reception of start command from central test program, the software enables the output. But the output will not start until the pattern edge trigger arrives. This setup provides a flexible DDJ injection method, where DDJ amplitude and shape (location of DDJ lines in jitter histogram) can be programmed through the AWG.

The jitter injection method can be used for bit error rate test if peak-to-peak jitter at BER=10e-12 is less than 500ps because the Agilent 81133 can accommodate only +/-250ps jitter modulation. For total jitter more than 500ps, delay lines with wider modulation range have to be used.

3. Jitter Measurement Using Continuous Time Interval Analyzer (CTIA)

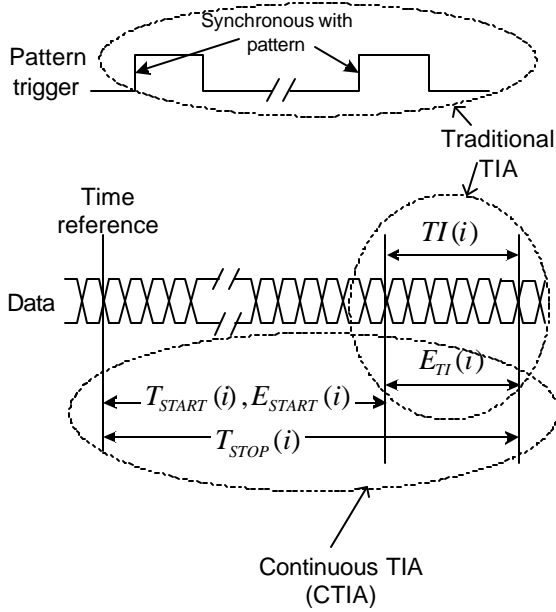


Figure 4: Continuous time interval analyzer (CTIA) - operation principle

Figure 4 shows the operation principles of the CTIA. The CTIA measures absolute time tags relative to a common reference rather than relative time difference between two events. A typical CTIA measures two tags for each arming event, one for a START and another for a STOP event. The CTIA generates the following information for each time interval between the START and STOP events:

- START time tag, $T_{START}(i)$, which indicates the START event absolute time relative to the common reference time.
- STOP time tag, $T_{STOP}(i)$, which indicates the STOP event absolute time relative to the common reference time.
- START event number, $E_{START}(i)$, which represents the number of events passed from the reference time to the START event. $E_{START}(i)$ is programmable.

Time interval event count, $E_n(i)$, which indicates the number of events between START and STOP edges, can also be programmed.

The CTIA is especially useful for measuring long-term phase modulation variations (very low frequency jitter or wander), and also for efficient implementation of jitter separation algorithms, as will be discussed in the following sections for RJ and DDJ measurements.

3.1. RJ Measurement

To measure RJ, a number of positive pulse widths are measured, where the start event is a rising edge and the stop event is the immediate following falling edge. The start event controller sets the number of events between the start of any two subsequent measurements to a multiple of the events in the pattern. This ensures that the data-dependent edge shift is the same for all the sampled edges, and therefore no DDJ component is present in the sampled edges. Since the probability distribution function (PDF) of the total jitter is the convolution of RJ, DDJ, and PJ, this sampling regime can be viewed as a DDJ deconvolution scheme. Subsequently, an estimate of unit interval (UI) is obtained as below:

$$UI = \frac{t(N) - t(0)}{E(N) - E(0)} \quad \text{Eqn. 1}$$

where N is the total number of samples. The function $t(i)$ is defined as the START time tag obtained for measured sample i , and the function $E(i)$ is defined as the event number for measured sample i . The UI estimate is used to obtain an ideal location for each edge, and consequently estimate the time interval error (TIE), which is defined as the difference between an edge location and its ideal location:

$$TIE(i) = t(i) - [E(i) - E(0)] \frac{patLen}{ppat} UI \quad \text{Eqn. 2}$$

TIE can be computed for both START and STOP edges of an interval. The START and STOP samples are effectively uniformly sampled, and therefore each can be passed through windowing and FFT function. The total noise floor for each FFT sequence is a biased estimate of RJ RMS value. To remove the bias, the RJ estimate has to be scaled to compensate for the windowing loss [11]. Windowing is essential to reduce the PJ sidebands impact in total noise floor power. This process can be viewed as a frequency domain deconvolution method. In this case, only two FFT sequences are computed, one for the rising edges (start events), and another for the falling edges

(stop events), which produce two RJ estimates. These estimates might not be the same due to different factors including statistical variations and also the difference between the circuitry generating rising edges and falling edges in the transmitter output drivers. Averaging the two RMS RJ estimates yields a final RJ estimate.

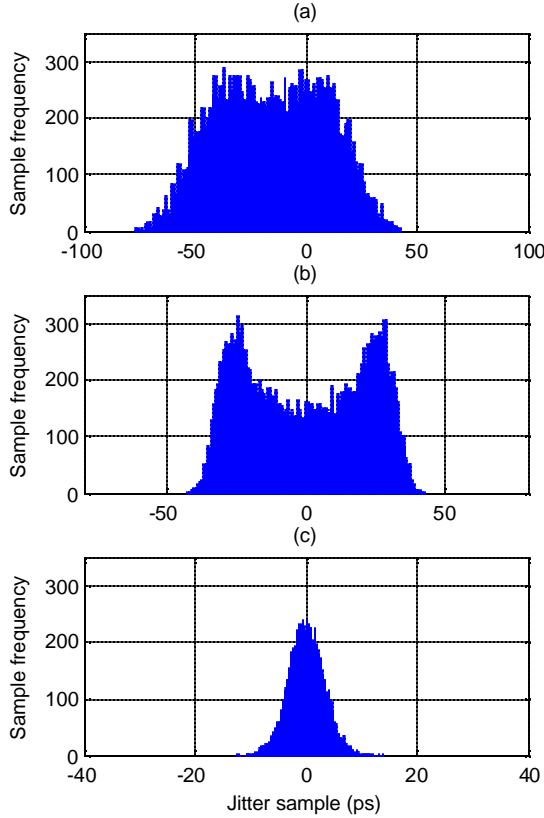


Figure 5: RJ separation example using DDJ/PJ deconvolution, bit rate=1Gbps, K28.5 pattern, $DDJ_{pp} = 26 ps$, $PJ_{pp} = 60 ps$, $RJ_{RMS} = 3 ps$ (Gaussian), (a) total jitter histogram before deconvolution, (b) jitter histogram after DDJ deconvolution, (c) jitter histogram after DDJ/PJ deconvolution.

The CTIA sampling rate is typically much less than the bit rate. If the jitter profile includes any high frequency PJ, aliasing will occur. This, however, does not impact RJ measurements because all PJ peaks are cancelled whether aliased or not.

Figure 5 shows the jitter histogram for simulated data that contains RJ, DDJ, and PJ. Plot (a) shows the histogram when samples are taken randomly, while plots (b) and (c) illustrate jitter histogram when

samples are taken on specific edges of the pattern (DDJ deconvolution), and after PJ is cancelled (PJ deconvolution), respectively. These plots demonstrate the ability of the method to extract RJ. Simulation shows that this method is capable of measuring RJ with very high precision, approximately 3% using 8192 edge samples. Proper choice of windowing function provides high degree of immunity to even large amounts of PJ (typically 25fs increase in RJ for 2ns PJ peak-to-peak at any frequency).

3.2. DDJ Measurement

For DDJ measurement, the start event sequence is selected such that the difference between each two consecutive start events is a multiple of pattern events plus 1. This allows measurement of jitter samples for all the edges in the pattern. Sufficient number of samples are taken to ensure between 100 and 1000 TIE samples are available for each pattern edge. The samples taken for each edge are averaged to attenuate the RJ and PJ components that are uncorrelated with the pattern. The remaining jitter represents DDJ. Special randomization techniques must be used to ensure that some low frequency PJ components with frequencies close to the CTIA sampling rate do not inflate the DDJ estimate. The peak-to-peak DDJ is estimated by subtracting the maximum and minimum of the edge DDJ.

The repeatability of DDJ measurements using the CTIA can be estimated as below:

$$s_{DDJ} = \frac{\sqrt{2(s_{RJ}^2 + s_{PJ}^2)}}{\sqrt{M}} \quad \text{Eqn. 3}$$

where M is the number of samples per pattern edge, and s_{RJ} and s_{PJ} are the RMS values of RJ and PJ. This relation follows from the averaging operation performed for each pattern edge. Eqn. 3 shows that DDJ measurement repeatability is inversely proportional to \sqrt{M} .

4. Jitter Injection Verification

We used oscilloscopes to verify the jitter injection setup described in Section 2 and also validate the accuracy of CTIA-based jitter algorithms. In this section, we describe how to use high-bandwidth equivalent-time (ET) digital sampling oscilloscope (DSO) for DDJ measurement, and real-time (RT) DSO for RJ and PJ measurement. We use the Tektronix

CSA11801C as the ET-DSO with 20GHz analog bandwidth and sampling rate of 200kHz, and the Tektronix TDS7404 as the RT-DSO with 4GHz of analog bandwidth and 20Gs/s sampling rate. The ET-DSO is the instrument of choice for DDJ measurement because of its high front-end bandwidth, which minimizes the instrument impact on DDJ. For PJ measurement, however, the RT-DSO is a more suitable tool, especially for mid to high frequency PJ, because it yields edge location information for many adjacent edges. In addition, the limited bandwidth of the RT-DSO relative to the ET-DSO does not impact PJ measurement because PJ energy is concentrated around the signal main harmonic, which is well within the DSO passband for bit rates up to 3.25Gbps (main harmonic at 1.625GHz). For RJ measurement, some references recommend the use of ET-DSO due to its low noise floor. We use the RT-DSO for measuring RJ more than 3ps because: (i) the internal RJ of the oscilloscope does not reduce the measurement accuracy significantly, and (ii) the RT-DSO allow implementation of frequency-domain RJ deconvolution method, which is robust against the effects of PJ on RJ accuracy and precision.

4.1. DDJ Measurement

ET-DSO is the ideal instrument to measure DDJ because of its high-bandwidth, and near linear phase response (low group delay variations). ET-DSO requires a trigger signal synchronous with the pattern to estimate average locations of all pattern edges relative to each other. The pattern trigger signal is either supplied by the transmitter, or has to be generated by a clock recovery circuit. We used the former. The pattern edge location estimation consists of two steps:

1. Coarse edge locator. An automated program locates all the edges in a single repetition of pattern using DSO trigger delay feature and threshold crossing estimation tools of the oscilloscope.
2. Fine edge locator: The coarse edge location estimates are used to adjust the DSO trigger delay to ensure an edge can be displayed on the DSO with horizontal and vertical scales set to minimum. This allows edge location estimation with highest accuracy that the DSO provides.

The edge location estimates are used to estimate unit interval (UI), and subsequently each edge shift relative to their ideal location. This method, however, requires measurement of thousands of voltage

samples to collect enough statistics for each edge. Even for moderate number of pattern edges (e.g., 64 for 127-bit PRBS7) and a fully automated procedure, a single DDJ measurement might take several tens of seconds to complete. A recent method from Agilent Technologies[12] reduces the total number of required samples for single edge detection through signal modeling and interpolation, which can increase DDJ measurement speed significantly.

4.2. PJ/RJ Measurement

To validate PJ injection, we have used a real-time sampling oscilloscope (TDS7404). This oscilloscope allows acquisition of up to 40us data record with sampling rate of 20Gs/s. The front-end bandwidth is 4GHz. To extract PJ, we use cubic spline interpolation to estimate the edge timing, which is the time at which the signal crosses a given threshold (usually 50% of the signal peak-to-peak). The extracted edge timings are used to estimate UI and subsequently time interval error (TIE) sequence in a similar way given by Eqn. 1 and Eqn. 2. The TIE sequence is interpolated for missing edges because NRZ data signals do not have transitions between two bits of the same polarity. The interpolated TIE sequence is passed through windowing and FFT to represent the signal in the frequency domain. The PJ components appear as distinct peaks in the FFT sequence. For the data signals with repeating short patterns (typically less than 127 bits), the DDJ (due to both the signal under test and the DSO) can also result in distinct peaks in FFT sequence at frequencies that are multiple of pattern repetition rate [2]. Such components are considered DDJ and ignored for PJ estimation.

Some methodologies use the inverse FFT of the DDJ spectral lines to estimate the total DDJ [2], and use the noise floor power as an estimate of random jitter. For longer PRBS type patterns, however, DDJ energy distributes over many frequency bins and mostly contributes to the noise floor instead of appearing as FFT peaks, which degrades the accuracy of DDJ and RJ estimates. Instead, we use the following RJ estimation method that is not sensitive to DDJ.

For RJ measurement, the same procedure as above is used to estimate TIE sequence for all the existing edges in the acquired signal. Knowing the pattern, the estimated edges are divided into multiple groups, each associated with the repetition of one specific pattern edge. Such grouping ensures that there is no pattern-dependent edge shift within the group. Each

group is then passed through windowing and FFT. The average noise floor power of these FFT sequences provides an estimate of RJ.

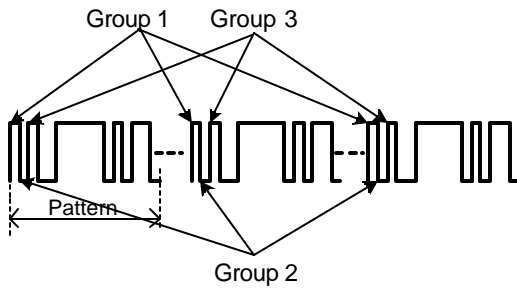


Figure 6: TIE grouping to eliminate DDJ impact on RJ measurement

5. Measurement Results

To validate the jitter injection methodology, we injected RJ, DDJ and PJ into a serial data stream and performed jitter measurement using the real time and equivalent time oscilloscopes, and the Femto 3200 CTIA. Figure 7 shows the RMS RJ measured using the TDS7404 RT-DSO from Tektronix and the GuideTech Femto 3000 CTIA; the vertical axis is in logarithmic scale because the noise generator attenuation is selected in db. Both instruments show that the injected RJ scales with the Gaussian noise level, resulting in expected linear relationship between the noise generator attenuation and the injected RJ. The DDJ and PJ deconvolution algorithm in Section 3 is used for both instruments. Figure 8 illustrates that the RJ measurement is not sensitive to different DDJ values injected; the variations in Figure 8 are within the statistical variations of the measurement. Figure 9 shows that the RJ measurements vary slightly as PJ is injected into the data stream. This is mainly due to the slight non-linearity of the Agilent 81133 delay line modulation, which reduces the noise power when the total variation become significant relative to the 250ps delay line modulation limit. The results also confirm the effectiveness of the frequency-domain deconvolution methods for the RJ estimation. RJ test times less than 50ms are achievable because of the CTIA optimized sampling and processing capability.

The DDJ is measured with the CSA11801C ET-DSO from Tektronix using the 20 GHz sampling heads to reduce the oscilloscope impact on the DDJ. The measurements in Figure 10 show that the DDJ increases proportionally with the amplitude of the AWG output, which validates the DDJ injection method. The DDJ is also measured with the GuideTech Femto 3200 CTIA using internal

calibration to remove the effects of CTIA bandwidth limitation. CTIA measurements match that of ET-DSO. The DDJ measurement with CTIA is much faster than ET-DSO. For a typical PRBS7 pattern with 64 edges, the CTIA can estimate the DDJ in less than 100ms, while the ET-DSO takes several minutes for the same number of edge samples.

Figure 11 illustrates that the CTIA-measured DDJ variations for different amounts of PJ is within expected statistical fluctuations, except for slight decrease in the DDJ for large values of the PJ, which is due to the non-linearity of the delay line modulator used. In addition, the DDJ measurement repeatability is within +/-1ps, which is sufficient for many testing applications.

The total RJ and DDJ measurement time with oscilloscopes is in the range of a few seconds (2s to 20s), whereas CTIA can complete the same measurement in 200ms to 500ms.

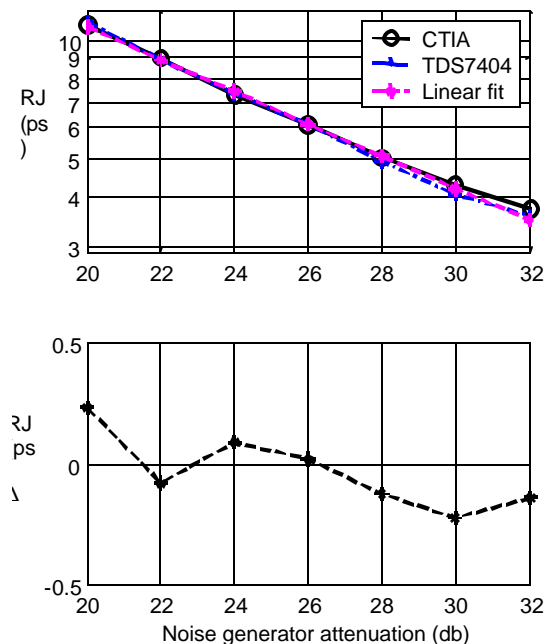


Figure 7: RJ injection and verification, bit rate = 2.5Gbps, K28.5 pattern

The results clearly show the effectiveness of the proposed jitter generation method to inject RJ, PJ, and especially DDJ in a controlled and independent fashion. The jitter measurement results also demonstrate ability of the CTIA to measure the RJ and DDJ very accurately in less than a few hundred

milliseconds, which is at least an order of magnitude faster than oscilloscopes measurements.

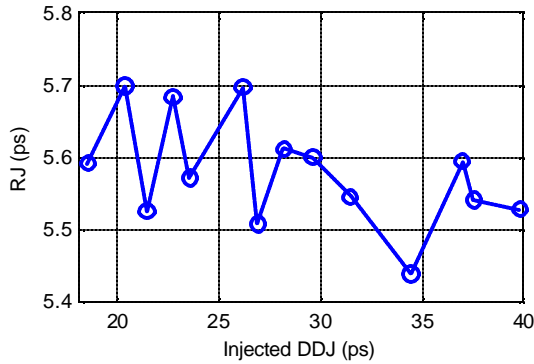


Figure 8: RJ insensitivity to DDJ, bit rate = 2.5Gbps, K28.5 pattern, noise generator attenuation = 27db

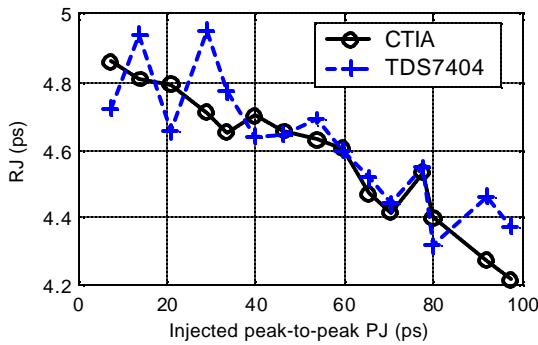


Figure 9: RJ variation due to PJ injection, bit rate = 2.5Gbps, K28.5 pattern

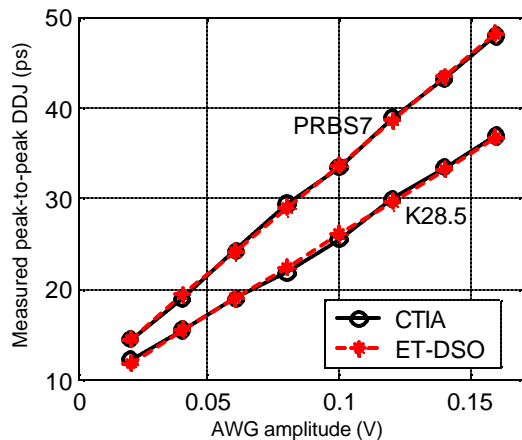


Figure 10: DDJ injection verification with ET-DSO and CTIA, bit rate = 2.5Gbps

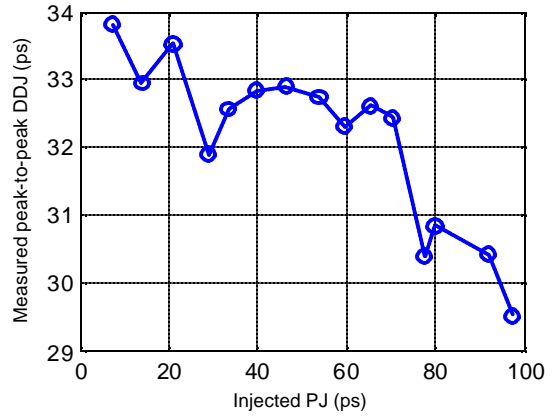


Figure 11: DDJ measurement in the presence of PJ, bit rate = 2.5Gbps, pattern K28.5.

6. Conclusions

We presented a delay line-based method for injection of programmable amounts of RJ, DDJ, and PJ jitter in a data stream. Specific advantages of the setup are the injection of large values of RJ, and the DDJ control without using DDJ injection filters. This setup can be used for the test of multi-Gbps data communication receivers, such PCI-Express, FiberChannel, Serial ATA, etc. We also presented oscilloscope-based jitter measurement methodologies for verification of jitter injection techniques. Equivalent-time sampling oscilloscope is used for DDJ measurement, while real time sampling oscilloscope is selected for RJ and PJ verification.

Although sufficient for characterization and verifications, DSOs are typically slow for production testing. We introduced the concept of continuous time interval analyzer (CTIA) and presented associated algorithms to optimize the number of samples required for jitter measurement, and provide fast, precise, and accurate estimates of RJ, and DDJ without using any hardware generated pattern trigger signal. CTIA, in essence provide an embedded or virtual pattern marker capability. Repeatable and fast CTIA measurements make it a strong candidate for production jitter testing.

References

- [1] "Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method & Physical Layer Specifications, XGMII Extended Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)", IEEE Draft P802.3ae/D3.3, October 2001.

- [2] National Committee for Information Technology Standardization (NCITS), “*Fiber Channel Methodologies for Jitter and Signal Quality Specification (MJSQ)*”, T11.2/Project 1316-DT/Rev 10.0, March 2003.
- [3] “*Infiniband Architecture, Chapter 6: High Speed Electrical Signaling - 2.5Gb/s Physical Specifications*” Release 1.0, Vol.2, October 2000.
- [4] Y. Cai, S. A. Werner, G. J. Zhang, M. J. Olsen, R. D. Brink, “*Jitter Testing for Multi-Gigabit Backplane SerDes - Techniques to Decompose and Combine Various Types of Jitter*”, International Test Conference, 2002, pp 700-709.
- [5] Y. Cai, B. Laquai, K. Luehman, “*Jitter testing for gigabit serial communication transceivers*”, IEEE Design and Test of Computers, pp 66-74, January 2002.
- [6] T. Yamaguchi, et al, “*Effects of deterministic jitter in a cable on jitter tolerance measurements*”, International Test Conference, 2003, pp 58-66.
- [7] T. Yamaguchi and M. Soma, “*Extraction of peak-to-peak and RMS sinusoidal jitter using an analytic signal method*”, IEEE VLSI Test Symposium, 2000, pp. 395-402.
- [8] Agilent Technologies, “*Measuring jitter in digital systems*”, Application note 1448-1.
- [9] J. Wilstrup, “*A method of serial data jitter analysis using one-shot time interval measurements*”, International Test Conference, 1998, pp 819-823.
- [10] M. P. Li, J. Wilstrup, R. Jessen; D. Petrich; “*A new method for jitter decomposition through its distribution tail fitting*”, International Test Conference, 1999, pp 788-794
- [11] E C. Efeachor and B. W. Jervis, “*Digital Signal Processing A Practical Approach*”, Addison-Wesley Publishing Inc., 1993
- [12] “*Jitter separation – 50 Mb/s to Over 40Gb/s using the Agilent 86100C Infiniium DCA-J*”, Agilent Technology white paper.