

# Bounded Uncorrelated Jitter (BUJ) Characterization Platform for High-Speed Interconnects

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## ABSTRACT

As inter-chip data rates move towards the Gbps regime, effects such as jitter that may have been ignored at lower data rates are becoming significant [1,2]. For example, the reduction of the I/O interconnects timing budget [3] places a stringent requirement on the total jitter budget. Jitter can be divided into different subcomponents, each with different root causes and properties [4]. Bounded Uncorrelated Jitter (BUJ), a jitter subcomponent, is partially caused by coupling from on-chip sources, or crosstalk coupling of signals switching from adjacent interconnects on printed-circuit boards (PCB) [5]. However, the characteristics of BUJ are still ill understood [6]. To study the characteristics of BUJ due to board-level coupling, we developed a test platform. Our experimentation platform involved the design and manufacture of PCB traces to instantiate high-speed interconnects, the setting up of a measurement system and post-processing algorithms to analyze the measured data.

### PCB Design:

Figure 1 shows the physical three-dimensional view of the PCB used in our experimental setup. It includes multiple traces on a FR4 PCB, which allow investigation of coupling impact on jitter. The thickness of the FR4 substrate, the copper trace width and the trace thickness were selected based on the PCB manufacturer's capabilities as well as to satisfy the characteristic impedance. The copper trace thickness,  $1.68\text{mils}$ , and substrate thickness,  $10\text{mils}$ , are limited by the selected manufacturer's capabilities. Note that  $1\text{mil}$  is equal to  $0.0254\text{mm}$ . For a dielectric constant of  $4.0$  and a characteristic impedance of  $50\Omega$  the width of the trace is calculated to be approximately  $17\text{mils}$ .

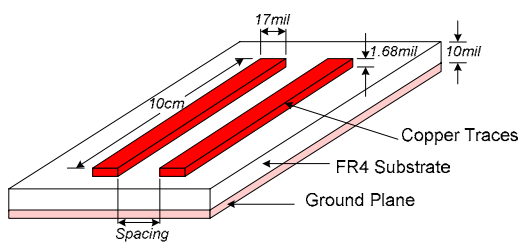


Figure 1: PCB Dimensions

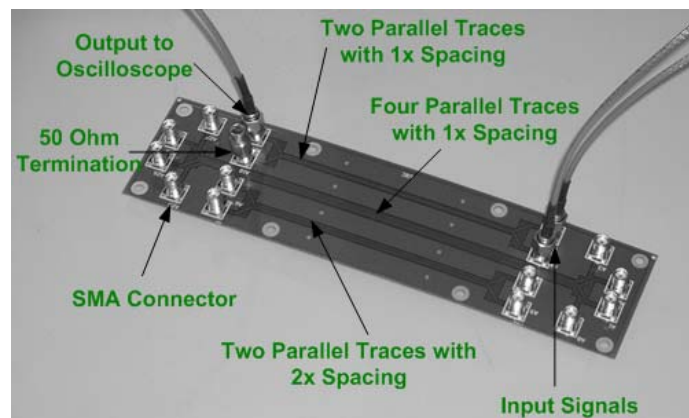


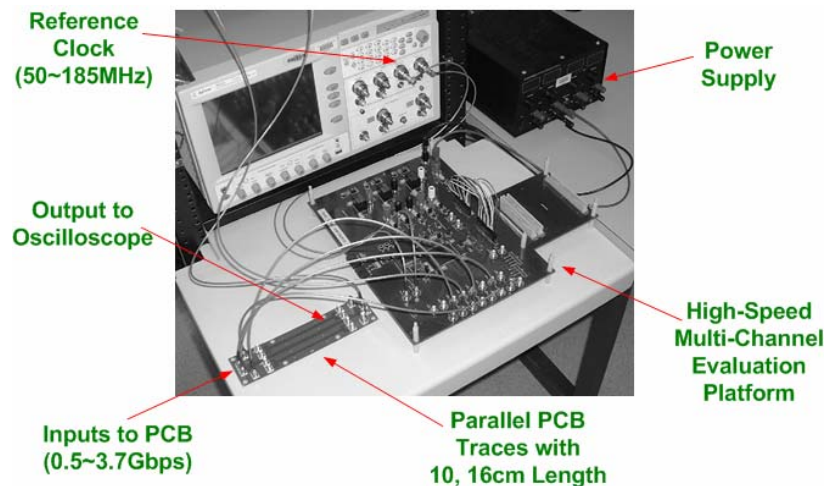
Figure 2: Photograph of a Manufactured PCB

Figure 2 shows the manufactured version of the PCB design. On this PCB, there are three different sets of parallel traces. The top and bottom set have only two parallel traces each. The spacing between the two traces on the top of Figure 2 is labeled as  $1 \times \text{Spacing}$ , to indicate that the distance between the two adjacent traces is equal to one time the width of the trace. In this paper,  $1 \times \text{Spacing}$  is equal to  $17\text{mils}$  trace width mentioned earlier. Similarly, the bottom set has a spacing of  $2x$ . Both ends of the parallel traces are accessible through SMA connectors. The middle set of four parallel traces in Figure 2 has a  $1 \times \text{Spacing}$  between traces. On the right hand

side of the figure, the signal sources are connected to both traces through SMA connectors. In this setup, one trace acts as the *aggressor* and the other acts as the *victim* trace. On the left hand side of the figure, the victim trace is connected to an oscilloscope to observe the victim signal behavior at the far end while the aggressor trace is simply terminated by a  $50\Omega$  termination.

### **Measurement Setup:**

Our measurement setup uses a high-speed evaluation platform to provide multi-channel signals. Figure 3 shows this setup. Lattice Semiconductor's high-speed multi-channel evaluation platform, *ORT82G5 Evaluation Board*, was used as the signal source. Because the evaluation platform requires a differential reference clock signal to adjust the data rates of the signal from the platform, the Agilent *86130A* is used as the differential reference clock to the board. As illustrated in Figure 3, four signal channels are connected from the evaluation platform to the PCB. The outputs of the PCB are connected to a real-time oscilloscope. A real-time oscilloscope is necessary to perform individual edge and transition analysis. In this work, an Agilent *Infiniium 54856* real-time sampling oscilloscope is used. Next, we will describe the post-processing algorithm to remove unwanted jitter based on the timing and amplitude data recorded from a real-time oscilloscope.



**Figure 3: Measurement Setup**

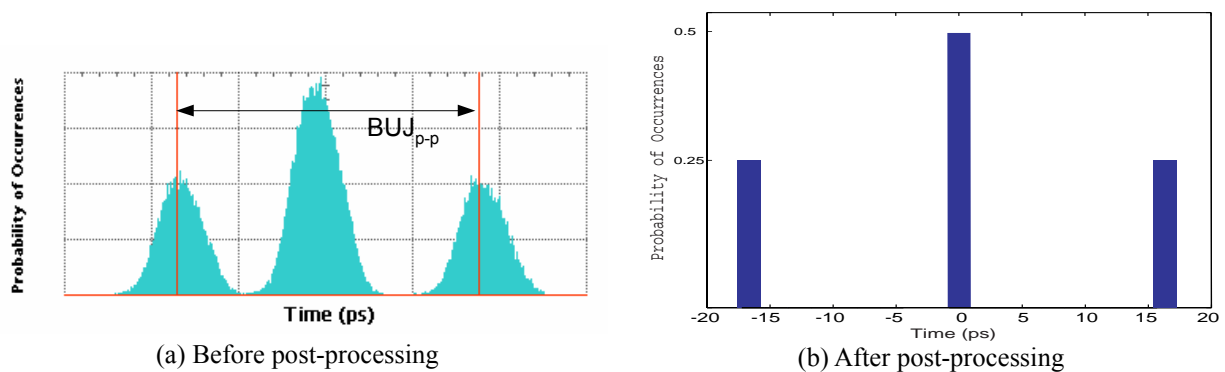
### **Data Post-Processing:**

In view of generating BUJ histograms, the recorded timing and amplitude data needs to be post-processed to remove unwanted jitter sources, such as Random Jitter (RJ), and high frequency Periodic Jitter (PJ), and edge transition glitches. A BUJ histogram is a diagram that plots the population of victim edge deviation from the ideal place due to BUJ. In jitter analysis, a measurement value that is the edge shift from the ideal place is usually in time units. In theory, when the number of samples approaches a large number, the normalized histogram provides a good estimate of the probability density function (PDF).

The edge crossing level is assumed to simply be half the amplitude of the victim signal. Because the recorded time and amplitudes do not necessarily match the edge crossing amplitude, interpolation is required to estimate the location of the edge crossings. Linear interpolation is applied to find the exact location. However, there exists other techniques such as  $\sin(x)/x$  and cubic-spline interpolation. Glitches also exist in the signal waveform due to amplitude noises. It can be removed by taking the mean of the glitch edge crossing times.

The jitter on a victim signal contains RJ and PJ components in addition to BUJ. If a non-clock type pattern is used, it will also contain a data-dependent jitter (DDJ) component. In our experiments, the victim trace is operated by a clock signal to eliminate DDJ effects. For removing the RJ and high-frequency PJ, the pattern edge jitter averaging technique is used; i.e., the victim edge time deviations are averaged for the edges that correspond to a different aggressor pattern bit. To perform this technique, it is necessary to ensure that the aggressor and victim

signal frequencies are synchronous. The synchronous assumption is valid in many practical cases such as multi-lane PCI-Express applications with a common clock. In this technique, an aggressor pattern is repeated many times and jitter on each edge is averaged for eliminating statistical Gaussian variations of RJ and periodic variations of PJ. As an example, Figure 4 (a) shows the jitter histogram measured with a real-time oscilloscope which includes RJ and possibly some small amount of PJ. In this experiment, the aggressor is running with a K28.5 [7] pattern and the clock signal is selected as the victim. The histogram of Figure 4 (a) is filtered by the averaging technique for obtaining the distribution of BUJ that appears as three delta-like function lines, as shown in Figure 4 (b). In the data from which part (b) was generated, only two parallel traces were considered and aggressors and victim were phase-aligned with respect to the timing edges. The left and right delta lines represent the effect of the aggressor's rising and falling edge on the victim's falling edge. The left delta line corresponds to the probability of a faster victim edge crossing due to this particular aggressor pattern. Conversely, the right delta line corresponds to the probability of a slower victim edge crossing. The middle delta line represents the probability of occurrence of the victim edge when the aggressor has no edge transition.

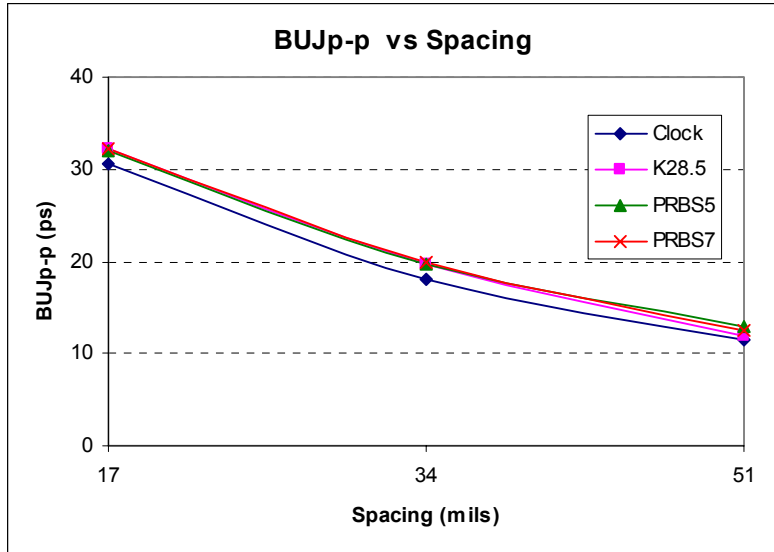


**Figure 4: Histograms Before and After Post-Processing**

### **Measurement Results:**

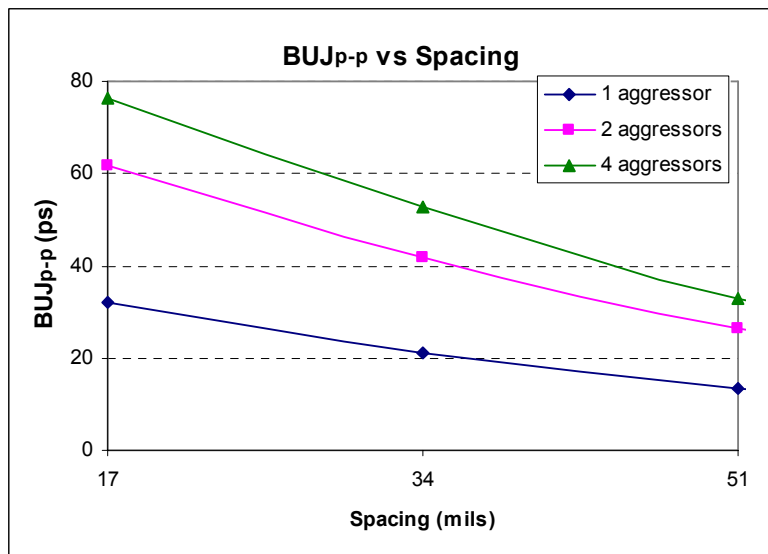
In this section, we use peak-to-peak BUJ,  $BUJ_{p-p}$ , to evaluate our measurements.  $BUJ_{p-p}$  is the absolute time from the left far-most peak to the right far-most peak or the left far-most delta line to the right far-most delta line. This is as illustrated in Figure 4 (a).

Figure 5 shows results for  $BUJ_{p-p}$  with different aggressor data patterns for one aggressor and one victim traces. Notice the trend of  $BUJ_{p-p}$  versus trace spacing. As the spacing between the adjacent traces increases, the BUJ effect decreases. The results for different data patterns show discrepancy. In particular, the clock data pattern has a smaller  $BUJ_{p-p}$ . This is due to the lack of aggressor data-dependent jitter (DDJ), which only occurs to data patterns that have consecutive '1's and '0's, as is the case for the aggressor signal generator of the other data patterns shown. As an example, K28.5 has a maximum of five consecutive '1's and '0's in its data pattern. In practical situations, it is important to take into consideration the effects of DDJ, which more frequently originates from the data sources and also less frequently from reflections in PCB traces. Figure 5 shows that the DDJ of the aggressor data pattern introduces an error of only  $2ps$  or less on our  $BUJ_{p-p}$  measurements with signals generated from the Agilent 86130A.



**Figure 5: Effect of Data Patterns on Peak-to-Peak BUJ**

Figure 6 illustrates an experiment of increasing the number of aggressor from one to two. For simplicity, the aggressor signals are all synchronized with the victim clock signal. Moreover, the victim trace is always sandwiched between two parallel traces. As the number of aggressor traces increases from one to two, the  $BUJ_{p-p}$  doubles. This is the case when both aggressors are operating with similar data pattern. However, two different aggressor PRBS data patterns can also double  $BUJ_{p-p}$ . As the number of aggressors increases beyond two, the  $BUJ_{p-p}$  increases but with lesser contribution from traces further away, hence, the cumulative effect of additional aggressor traces on  $BUJ_{p-p}$  is not linear.



**Figure 6:  $BUJ_{p-p}$  for Multiple Aggressors**

In high-speed interconnects, the signals in parallel traces may not have their edge crossings phase-aligned. In other words, time skew exists between the signals. Figure 7 illustrates the  $BUJ_{p-p}$  values obtained when changing the skew between one aggressor and one victim performed with Agilent 86130A. Also, the measurements were performed with different trace spacings of  $1x$ ,  $2x$ , and  $3x$ . The victim is a  $1GHz$  clock signal, and thus has a  $1000ps$

period. The skew is varied over one full period of the victim signal. The highest  $BUJ_{p-p}$  value occurs when there is no skew between the aggressor and victim signals. As the skew increases, the  $BUJ_{p-p}$  reduces. At about  $100ps$  time skew, there is almost no impact on the victim edges. In between  $100ps \sim 900ps$  time skew,  $BUJ_{p-p}$  is small because measurement results unavoidably include statistical residual error from RJ/PJ averaging. As the skew increases to  $900ps$ , the  $BUJ_{p-p}$  increases again. The maximum  $BUJ_{p-p}$  occurs again when the time difference matches one full period, i.e.,  $1000ps$ . Notice that as the spacing between traces increases from  $1x$  to  $2x$  and  $3x$ , the  $BUJ_{p-p}$  decreases as expected with the trend in Figure 5 ( $17mil = 1x$  Spacing,  $34mil = 2x$  Spacing, and  $51mil = 3x$  Spacing). Figure 7 can act as a guideline for designers to reduce  $BUJ$ . The transceiver can be designed to purposely avoid synchronous edge transitions of the signals from parallel traces. In other words, a time skew between signals can be introduced to minimize  $BUJ$ . As a result, the spacing between parallel traces can be minimized.

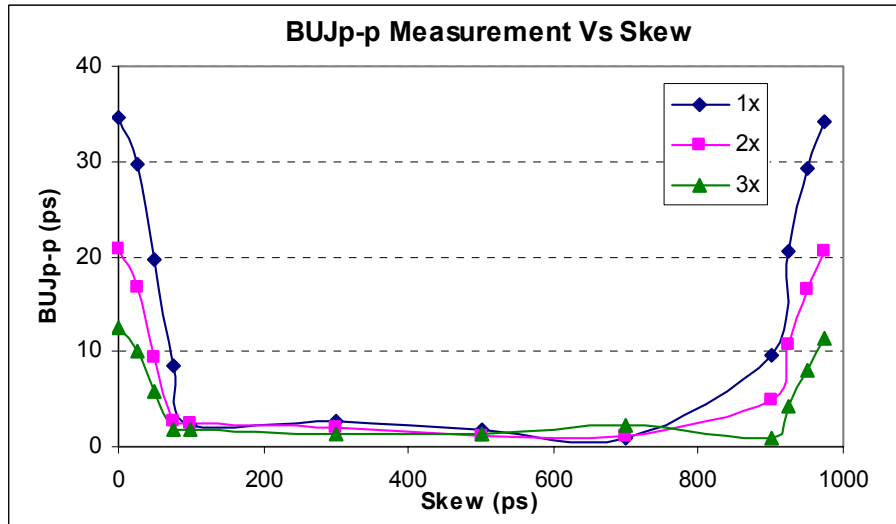


Figure 7:  $BUJ_{p-p}$  Vs Time Skew of a 1GHz Victim Signal

## Conclusions:

The design and manufacture of PCB traces instantiating high-speed interconnects, along with the measurement setup and post-processing algorithms we developed, have enabled us to explore the characteristics of  $BUJ$  further. Post-processing the measurement data successfully reduced RJs, and high-frequency PJs that we experienced. However, there are still  $2\sim 3ps$  of DDJ from the aggressor data pattern that cannot be avoided. These post-processed measurement results can reinforce simulations in order to enable the development of novel yet essential analytical models for  $BUJ$ . In this paper, we study the effect of different aggressor data patterns, increasing the spacing between traces, increase number of aggressors, and vary time skew between the aggressor and victims. This validates the platform we presented. With this platform,  $BUJ$  model can be developed to help engineers predict and understand the effect of  $BUJ$  on their design. In addition, the time skew measurement also acts as a guideline for designers to reduce  $BUJ$  and minimize spacing between parallel traces.

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